REMARKS

Applicant has added new claim 11 to round out the scope of the claims. Support for claim 11 may be found at least at page 21, line 13, through page 25, line 16, of applicant's specification. No new matter has been added.

Claims 1-10 stand rejected under 35 USC 102(b) on Vicard (U.S. Patent No. 5,708,715). Applicant respectfully traverses this rejection.

Applicant has amended claim 1 to recite "at least one non-volatile memory cell array block which is capable of receiving concurrent electrical erasure, the at least one nonvolatile memory cell array block comprising at least one main memory block region to store data, and at least one memory region configured to store a security release key corresponding to each of the at least one memory cell array block; at least one non-volatile storage unit configured to store a security registration lock corresponding to each of the at least one memory cell array block," as depicted in applicant's Fig. 1 and described at least at page 21, line 13, through page 25, line 16, of applicant's specification. Applicant has also amended claim 1 to no longer recite features which may have been construed as invoking 35 USC 112, paragraph 6. No new matter has been added.

Vicard does not disclose or suggest such features. Specifically, Vicard does not disclose a non-volatile memory cell array which has a first portion for storing data (such as user data) and a second portion for storing a security release key. The Examiner has cited the Functional Block 12, depicted in Fig. 1 of Vicard, as disclosing the non-volatile memory cell array recited in applicant's claim 1. Furthermore, the Examiner has cited the chip key signature stored in register 25 as disclosing the security release key of applicant's claim 1.

As depicted in Fig. 1 of Vicard, the register 25 is a part of the lock circuitry 11 and is not a part of the functional block 12, which may be used to store user data. Accordingly, even if the chip key signature did disclose applicant's security release key, it is not stored in the functional block 12, and therefore cannot disclose the features of claim 1 quoted above.

Additionally, one of ordinary skill in the art would not have been motivated to store the chip key signature in the functional block 12 of Vicard because the functional block 12 of Vicard is not enabled until the gating circuit 18 receives an enable signal from the comparison circuit 27. "When the gating circuit is fed with an enable signal on line 19, the external clock signal is passed on to the block 12 enabling its operation; in the absence of an enable signal on line 19, the block 12 is internally non-operational." (Vicard, col. 4, lines 38-42.) The enable signal is based on a comparison involving the chip key signature. Accordingly, if the chip key signature were stored in the functional block 12, the chip key signature could not compared to anything until the functional block 12 was activated, and the functional block 12 could not be activated until the chip key signature was compared. Due to this Catch-22 condition, such a device would be rendered non-operable.

In contrast, applicant's memory cell array block may be accessed regardless of a comparison, but the information may not be output from the memory cell array data output switching circuit until a comparison is made.

Claim 1 is therefore allowable. Claims 2-11 depend from claim 1 and are allowable due at least to their respective dependencies.

Claims 1-10 stand rejected under 35 USC 103(a) on Vicard in view of Chuang (U.S. Patent No. 6,031,757). Applicant respectfully traverses this rejection.

Chuang fails to overcome the deficiencies of Vicard noted above. Claim 1 is allowable for at least the reasons stated above.

Additionally, the combination of Vicard and Chuang does not disclose or suggest storing both a security release key and a security registration lock. As detailed at col. 5, lines 53-57, of Vicard, Fig. 2 depicts a register block 35 which replaces the register 25 depicted in Fig. 1.

Furthermore the single functional block 12 is replaced by multiple functional blocks 12A-12E. Fig. 2 is merely used to show that multiple functional blocks can be controlled. As shown in Fig. 2, the

register block is used to store signatures H(K1) – H(K6) which are respective hashes of chip keys K1-K6. These stored hashes are transmitted to the comparison block 27 to be compared with the IV2 values transmitted from the one-way hash function 26. The signal IV2 represents the one-way hash of a decrypted (IV1) input key K. Vicard does not disclose storing the IV2 signal at all, let alone in a non-volatile memory.

Furthermore, the Examiner has cited Chuang as disclosing the storing of a lock in a non-volatile memory. Applicant respectfully submits that the Examiner has misconstrued the disclosure of Chuang. The Examiner has merely cited to the Abstract of Chuang which discloses non-volatile memory cells that store sector lock signals and has apparently not realized that the disclosed sector lock signals have nothing to do with the lock and key features recited in claim 1. The sector lock signals of Chuang are not locks which correspond to keys, but rather, they are signals to indicate if a sector should be protected (or locked) against modification (col. 4, lines 14-62; and col. 6, line 17, through col. 8, line 10). Not only has the Examiner failed to provide any motivation to combine these very different technologies, the Examiner has also failed to show how the lock signal of Chuang could be combined with the purported lock of Vicard to achieve applicant's invention.

Neither Vicard nor Chuang discloses or suggest storing a security registration lock and a key as recited in claim 1.

Claim 1 is therefore allowable. Claims 2-11 depend from claim 1 and are allowable due at least to their respective dependencies.

Applicant solicits an early action allowing the claims.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. **299002053200**.

Dated: December 21, 2007

Respectfully submitted,

Adam Keser

Registration No. 54,217 MORRISON & FOERSTER LLP 1650 Tysons Blvd, Suite 400 McLean, Virginia 22102 (703) 760-7301